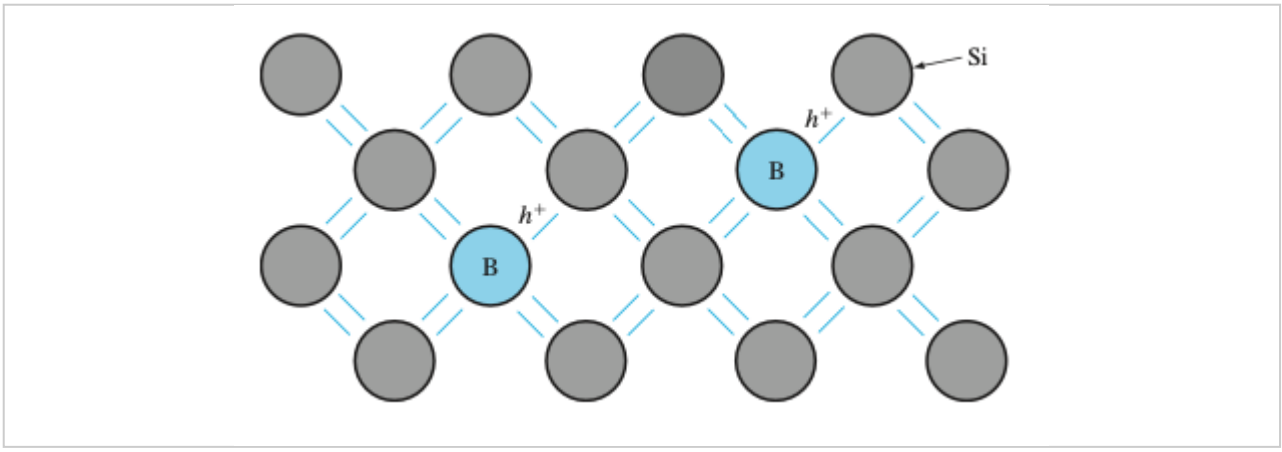
1



The simple schematic above illustrates a Si crystal at room temperature where some of the Si atoms have been replaced by a B atom. In this case, each of the dopant atoms have an electron less than the Si atoms, introducing an additional hole to the crystal.

How will the introduction of B atoms change the net charge of the crystal?
(correct: 2p, wrong: 0p, blank: 0p)
Select one alternative

- The B doping will not affect the net charge of the crystal ✔
- The B doping will make the crystal positively charged.
- The B doping will make the crystal negatively charged.

What do we typically call the kind of doping shown above?
(correct: 2p, wrong: 0p, blank: 0p)
Select one alternative

- Donor doping
- Blood doping
- Intrinsic doping
- Acceptor doping ✔

How would the introduction of B into a Si crystal be represented in a band diagram representation of the crystal?
(correct: 2p, wrong: 0p, blank: 0p)

Select one alternative

- The B doping will decrease the conduction band energy.
- B doping will decrease the Fermi energy in the system. ✔
- B doping will increase the band gap of the system.
- B doping will increase the mobility of the holes in the system.

Maximum marks: 6

2 Select the correct statements.
(correct: 2p, wrong: -2p, blank: 0p)
Select one or more alternatives:

- For Si, the mobility is higher for electrons than for holes ✔
- In a p-n junction, the conductivity is higher in the neutral region than in the depletion r ✔ on
- The conductivity in a semiconductor is independent of the doping concentration
- For Si, the lowest conductivity is obtained with zero doping

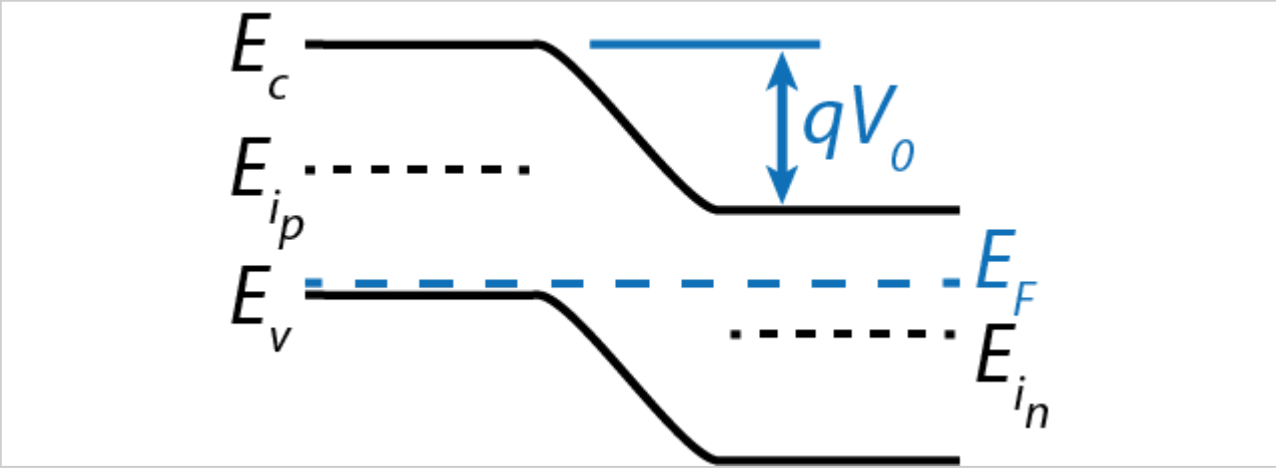
Maximum marks: 4

3 Which of the following experiments/measurements is best suited to determine the mobility of the majority carriers in a uniformly doped semiconductor sample:
(correct: 2p, wrong: 0p, blank: 0p)
Select one alternative:

- a C-V measurement
- the Stern–Gerlach experiment
- the Haynes-Shockley experiment
- the Hall effect experiment ✔

Maximum marks: 2

4



In the following we will consider a Si p-n junction at room temperature. The band diagram at thermal equilibrium for this junction is shown above.

Fill in the blanks in the following two sections of text. Words are suggested for each blank – choose the most appropriate one. (correct: 1p, wrong: -0.5p, blank: -0.5p, minimum score: 0p)

Within the depletion region in the p-type material, there is a net Select alternative (neutral, negative, positive)charge. This region is depleted of free Select alternative (acceptors, carriers, impurities, donors)and the remaining charge originates from the ionized Select alternative (electrons, acceptors, holes, donors). Moving further away from the junction into the neutral p-type material, we find a large number of free Select alternative (electrons, dopants, holes) and Select alternative (neutral, positive, ionized) acceptors. The concentration of charge carriers is Select alternative (less than, essentially equal to, larger than)that of the acceptors.

In the n-type material, there are electrons and Select alternative (ionized, very few, neutral, free) donors. In the neutral region, the Select alternative (entangled, immobile, free) electrons and the Select alternative (positive and immobile, positive and free, neutral and free, neutral and immobile) donors cancel out

with respect to charge. In the
depleted part of the n-type semiconductor, close to the junction, the semiconductor

has a net Select alternative (positive, neutral, negative) charge. Here, the semiconductor is

depleted of Select alternative (carriers, acceptors, donors) and the

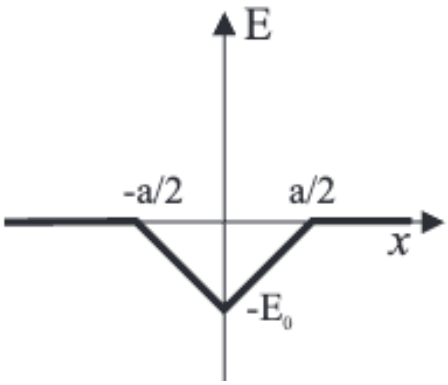
net charge is due to Select alternative (holes, ionized acceptors, unionized donors, ionized

donors). In this particular p-n junction, the doping is highest Select alternative (on the n-side, in the middle, on the p-side, at the gym). As a result, the current at the junction will be dominated by

Select alternative (electrons, acceptors, holes, donors) when the device is under forward bias.

Maximum marks: 14

5 A p-n junction has the E-field profile shown below. Determine the contact potential V_0 and the space charge density $\rho(x)$ as a function of a and E_0.



Space-charge density:
(correct: 4p, wrong: 0p, blank: 0p)
Select one alternative:

- $\rho(x) = \begin{cases} 0 \text{ for } x < \frac{-a}{2} \\ \frac{-4\epsilon E_0}{a} \text{ for } \frac{-a}{2} < x < \frac{a}{2} \\ 0 \text{ for } x > \frac{a}{2} \end{cases}$
- $\rho(x) = \begin{cases} \frac{2\epsilon E_0}{a} \text{ for } x < \frac{-a}{2} \\ 0 \text{ for } \frac{-a}{2} < x < \frac{a}{2} \\ \frac{-2\epsilon E_0}{a} \text{ for } x > \frac{a}{2} \end{cases}$
- $\rho(x) = \begin{cases} 0 \text{ for } x < \frac{-a}{2} \\ \frac{-2\epsilon E_0}{a} \text{ for } \frac{-a}{2} < x < 0 \\ \frac{2\epsilon E_0}{a} \text{ for } 0 < x < \frac{a}{2} \\ 0 \text{ for } x > \frac{a}{2} \end{cases}$ ✔
- $\rho(x) = \begin{cases} 0 \text{ for } x < \frac{-a}{2} \\ \frac{2\epsilon E_0}{a} \text{ for } \frac{-a}{2} < x < 0 \\ \frac{-2\epsilon E_0}{a} \text{ for } 0 < x < \frac{a}{2} \\ 0 \text{ for } x > \frac{a}{2} \end{cases}$

Contact potential:
(correct: 4p, wrong: 0p, blank: 0p)

Select one alternative:

- $V_0 = \frac{4E_0}{a}$
- $V_0 = \frac{aE_0}{4}$
- $V_0 = \frac{2E_0}{a}$
- $V_0 = \frac{aE_0}{2}$ ✔

Maximum marks: 8

6 *Fill in the blanks in the text below. Words are suggested for each blank – choose the most appropriate one. (correct: 1p, wrong: -0.5p, blank: -0.5p, minimum score: 0p)*

A p-n junction is operating under a certain reverse bias. If the reverse bias voltage is increased by a factor 3, what will be the impact on the following parameters?

- The depletion width will Select alternative (Remain unchanged, Decrease, Increase)
- The contact potential will Select alternative (Remain unchanged, Decrease, Increase)
- The junction capacitance will Select alternative (Decrease, Increase, Remain unchanged)
- The probability of breakdown will Select alternative (Decrease, Remain unchanged, Increase)

Maximum marks: 4

7 An abrupt Si junction (area = 0.0001 cm2) has the following parameters:
$N_d = 5 \cdot 10^{17} \mathrm{cm}^{-3}$
$N_a = 1 \cdot 10^{17} \mathrm{cm}^{-3}$

Given: $\epsilon_r = 11.8$

In thermal equilibrium:
What is the built-in potential (contact potential)?
(correct: 4p, wrong: 0p, blank: 0p)

Answer: [ ] (0,8 - 0,9) V

What is the total number of ionized acceptors in the depletion region?
(correct: 4p, wrong: 0p, blank: 0p)

Answer: [ ] (9,2 - 9,9) $\cdot 10^7$

Maximum marks: 8

7 - Abrupt Si junction (numerical answers)

The contact potential of the abrupt Si junction is given by

$$\begin{aligned} V_0 &= \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2} \\ &= (0.0259\,\mathrm{V}) \cdot \ln \frac{1 \cdot 10^{17}\,\mathrm{cm}^{-3} \cdot 5 \cdot 10^{17}\,\mathrm{cm}^{-3}}{(1.5 \cdot 10^{10}\,\mathrm{cm}^{-3})^2} \\ &= 0.856\,\mathrm{V}. \end{aligned} \tag{1}$$

We can find the total number of ionized acceptors in the depletion region by multiplying the acceptor concentration by the area of the volume of the depletion region on the p-side of the junction.

We first find the depletion region width using

$$\begin{aligned} W &= \left[\frac{2\epsilon V_0}{q} \left(\frac{1}{N_a} + \frac{1}{N_d} \right) \right]^{\frac{1}{2}} \\ &= \left[\frac{2(11.8 \cdot 8.85 \cdot 10^{-14}\,\mathrm{F\,cm}^{-1}) \cdot (0.856\,\mathrm{V})}{(1.6 \cdot 10^{-19}\,\mathrm{C})} \left(\frac{1}{(1 \cdot 10^{17}\,\mathrm{cm}^{-3})} + \frac{1}{(5 \cdot 10^{17}\,\mathrm{cm}^{-3})} \right) \right]^{\frac{1}{2}} \\ &= 1.158 \cdot 10^{-5}\,\mathrm{cm}. \end{aligned} \tag{2}$$

The depletion region extends x_{p_0} into the p-side of the junction,

$$\begin{aligned} x_{p_0} &= \frac{W}{1 + N_a/N_d} \\ &= \frac{(1.158 \cdot 10^{-5}\,\mathrm{cm}.)}{1 + (1 \cdot 10^{17}\,\mathrm{cm}^{-3})/(5 \cdot 10^{17}\,\mathrm{cm}^{-3})} \\ &= 9.65 \cdot 10^{-6}\,\mathrm{cm}. \end{aligned} \tag{3}$$

We can now calculate the number of ionized acceptors,

$$\begin{aligned} \text{number of acceptors} &= x_{p_0} A N_a \\ &= (9.65 \cdot 10^{-6}\,\mathrm{cm}) \cdot (0.0001\,\mathrm{cm}^2) \cdot (1 \cdot 10^{17}\,\mathrm{cm}^{-3}) \\ &= 9.65 \cdot 10^{7}. \end{aligned} \tag{4}$$

8 Diode Equation

The current in a p-n junction is described by the diode equation

$$I = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)(e^{qV/kT} - 1) = I_0(e^{qV/kT} - 1)$$

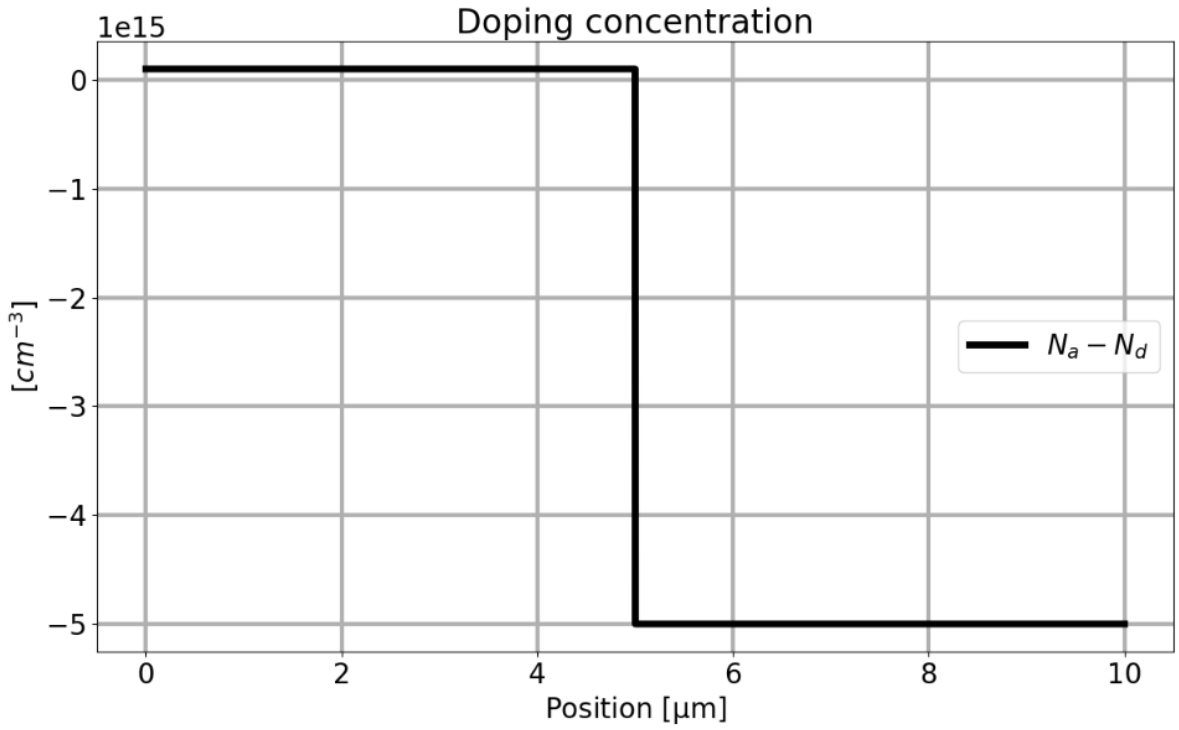
What assumptions have been made in the derivation of this equation?
(correct: 1p, wrong: -1p, blank: 0p, minimum score: 0p)

Select one or more alternatives

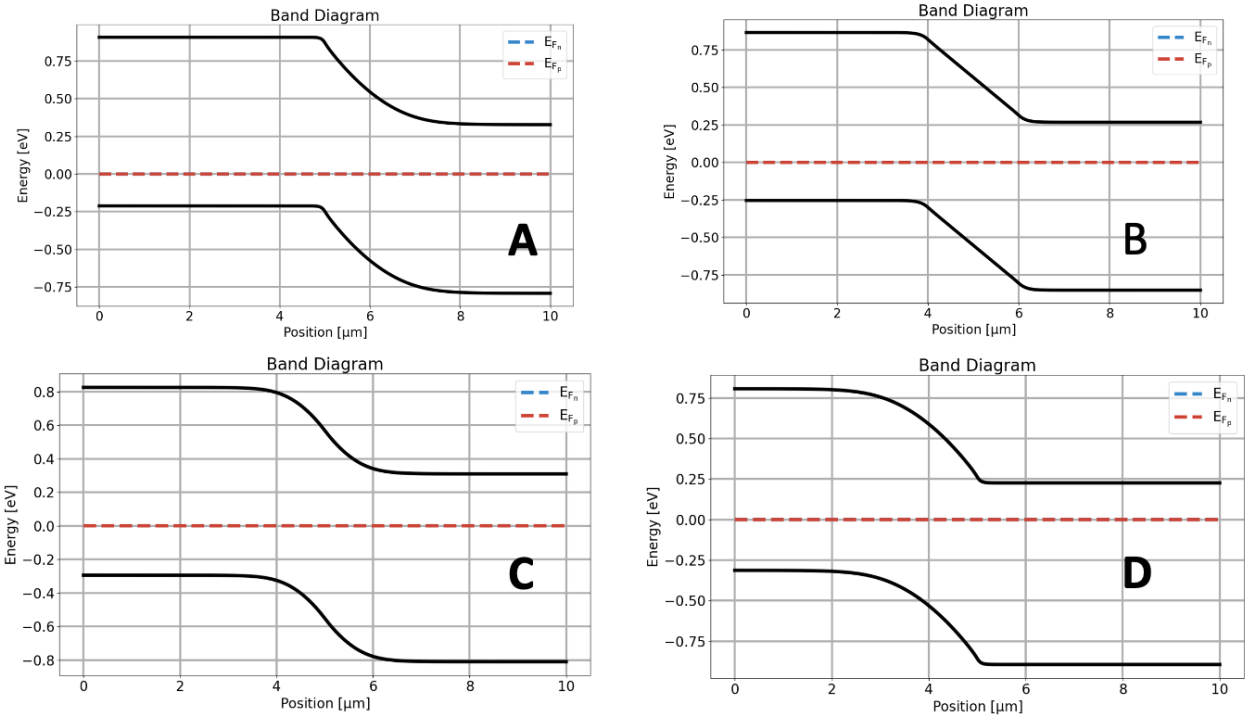
- [x] Assume low-level injection ✔
- [ ] Assume high-level injection
- [ ] Neglect drift of minority carriers
- [x] Assume abrupt p-n junction ✔
- [ ] Neglect diffusion of minority carriers
- [x] Recombination and generation in the transition region (depletion region) is neglected ✔
- [ ] Neglect variations in the width of the depletion region with the bias voltage
- [x] Neglect voltage drop across the neutral regions ✔

Maximum marks: 4

9 The figure below shows the doping profile $N_a - N_d$ for a p-n junction.



Which of the band diagrams shown below corresponds to a p-n junction with this doping profile?
(correct: 2p, wrong: 0p, blank: 0p)

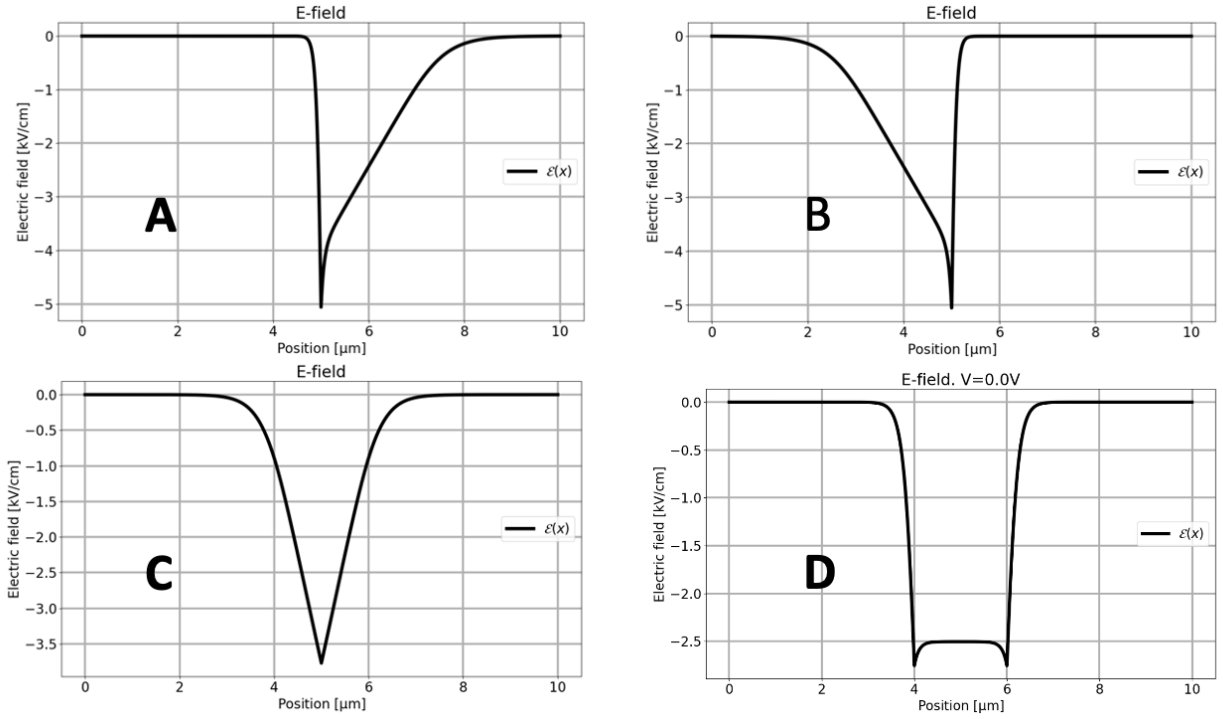


Select one alternative

- D ✔
- C
- A
- B

Which of the electric field profiles shown below corresponds to a p-n junction with this doping profile?

(correct: 2p, wrong: 0p, blank: 0p)

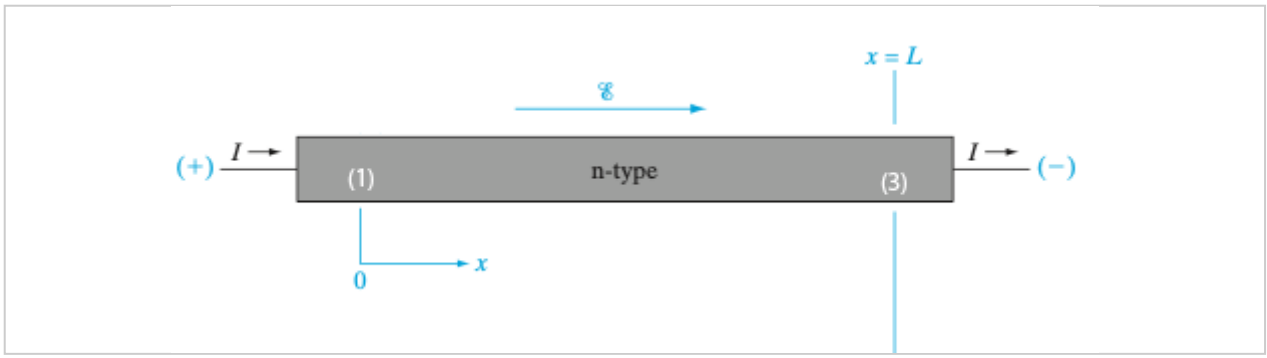


Select one alternative:

- A
- D
- C
- B ✔

Maximum marks: 4

10



Fill in the blanks in the text below. Words are suggested for each blank – choose the most appropriate one. (correct: 1p, wrong: -0.5p, blank: -0.5p, minimum score: 0p)

In an n-type bar which contains an electric field, as shown in the figure, the basic principles of the Haynes-Shockley experiment are as follows:

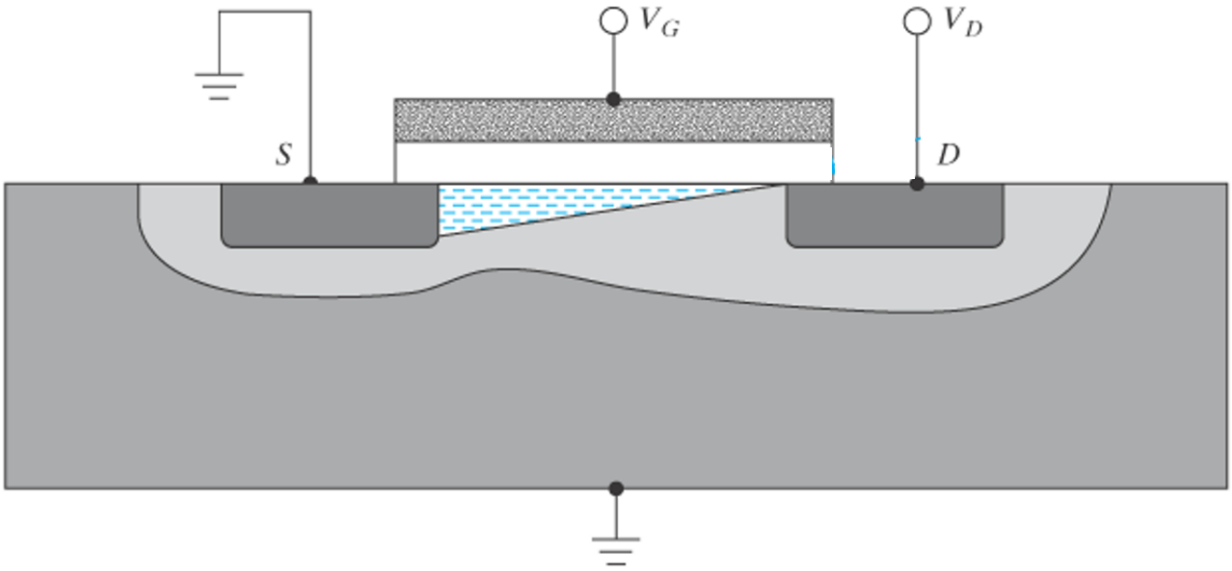
1. A pulse of [Select alternative] (electrons, holes) is created close to one side of the bar (1).

2. As the pulse [Select alternative] (drifts, diffuses) along the bar in the direction of the electric field, it spreads out due to [Select alternative] (diffusion, drift).

3. At the other end of the bar (3), we measure the width of the pulse to calculate the [Select alternative] (diffusion coefficient, concentration, mobility, carrier type)of [Select alternative] (majority carriers, minority carriers). We also measure the drift time of the pulse to calculate the [Select alternative] (mobility, carrier type, diffusion coefficient, concentration) of [Select alternative] (majority carriers, minority carriers).

Maximum marks: 7

11



The figure above shows the cross section of an enhancement mode (normally off) n-channel MOSFET at the onset of saturation.

Based on the indicated depletion region and inversion layer, select the correct voltage relationships.

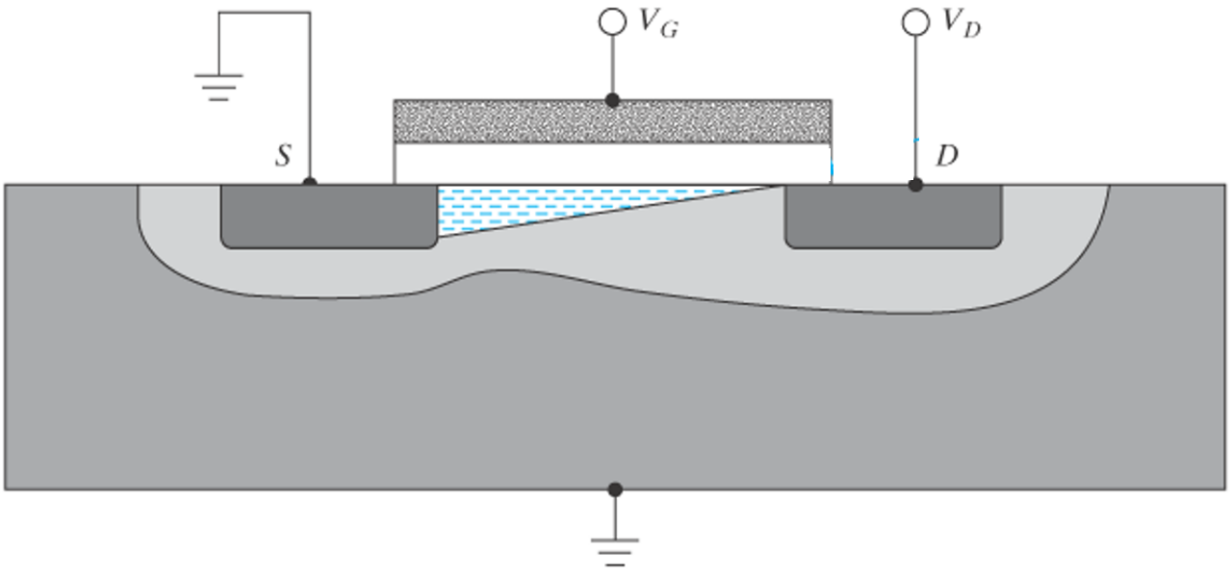
(correct: 2p, wrong: -2p, blank: 0p, minimum score: 0p)

Select one or more alternatives:

- ☐ $V_G > V_T$ ✔
- ☐ $V_D = V_G - V_T$ ✔
- ☐ $V_G \approx 0\text{V}$
- ☐ $V_G < V_T$
- ☐ $V_D \approx 0\text{V}$

Maximum marks: 4

12



What will typically be true for a MOSFET with a pinched-off channel?
(correct: 2p, wrong: 0p, blank: 0p)
Select one alternative:

- The drain current is close to zero ($I_D \approx 0$).
- There is a significant drain current, I_D. ✔
- The device is in the "OFF" state.
- The device is about to break down.

Maximum marks: 2

13 The threshold voltage of a MOS transistor is given by
$V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$ **(1)**.

QUESTION 1

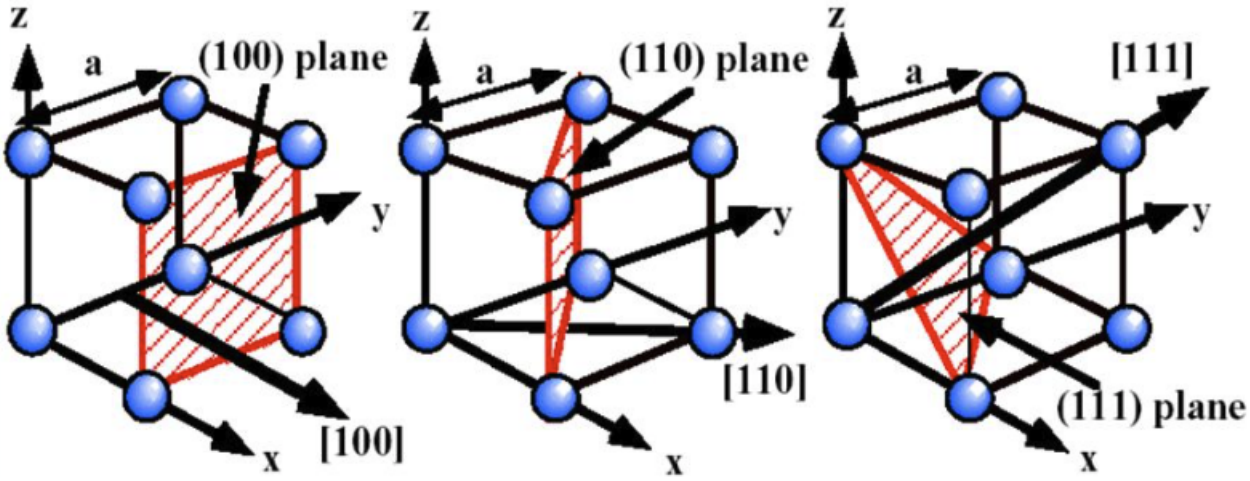
For an NMOS transistor, what will happen to the absolute value of the different terms in **(1)** if the doping concentration in the substrate is increased by a factor 2?

(correct: 2p, wrong: 0p, blank: 0p)

Select one alternative:

- $|\Phi_{ms}|$ decrease, $|\phi_F|$ increase, $|Q_d|$ increase
- $|\Phi_{ms}|$ increase, $|\phi_F|$ increase, $|Q_d|$ increase ✔
- $|\Phi_{ms}|$ increase, $|\phi_F|$ increase, $|Q_d|$ decrease
- $|\Phi_{ms}|$ increase, $|\phi_F|$ decrease, $|Q_d|$ decrease

QUESTION 2



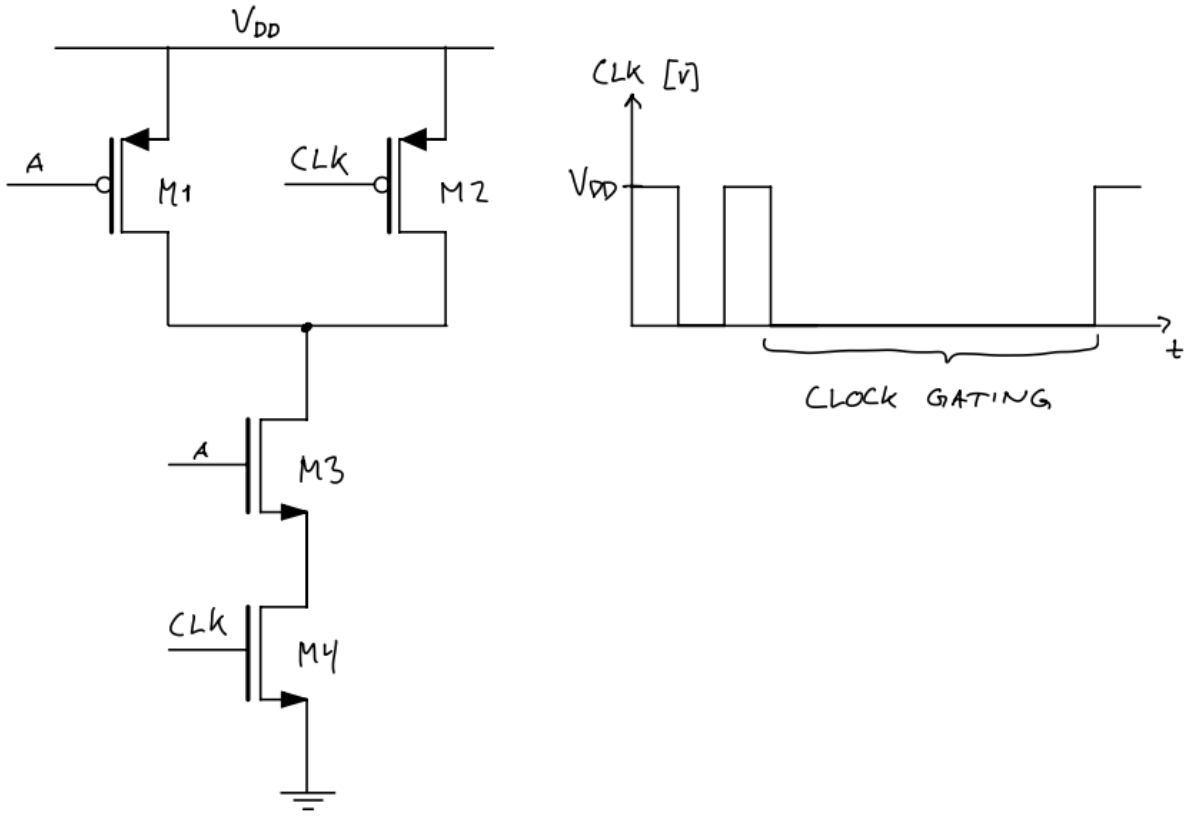
The figure above shows an illustration of a cubic crystal lattice with the {100} plane, {110} plane and the {111} plane indicated. Considering the properties of MOS transistors, what is the main reason why silicon ingots used for fabrication of integrated circuits are grown along the <100> direction?

(correct: 2p, wrong: 0p, blank: 0p)

Select one alternative:

- With {100} Si, the direction of the transistor current will be orthogonal to a {110} plane, causing less scattering and higher electron mobility than for {111} Si.
- Large silicon crystals are easiest to grow along the <100> direction, causing a more reliable fabrication process
- With {100} Si, the work function difference is smaller, causing better control of the threshold voltage.
- Using {100} Si results in a lower density of interface charge at the Si-SiO2 interface which will reduce the threshold voltage of both NMOS and PMOS transistors ✔

QUESTION 3



Clock gating is a popular technique used to save dynamic power consumption in digital integrated circuits, where the clock signal is disabled for circuits that is not in use. The figure above shows the schematic of a NAND-gate with the two input signals "A" and "CLK". During clock gating, the CLK signal remains at zero volt for a long period of time, and the PMOS transistor M2 will have a strong electric field across the gate oxide. As a consequence, there will be a current of carriers tunneling through the oxide barrier and some of the positive charge carriers will get trapped inside the gate oxide. The concentration of positive trapped charges inside the oxide will increase over time, an effect known as Negative-bias temperature instability.

What could be the consequence of this accumulation of trapped positive charges in the gate oxide?

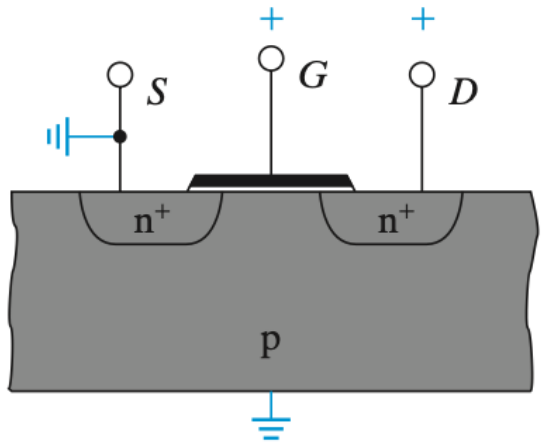
(correct: 2p, wrong: 0p, blank: 0p)

Select one alternative:

- The hole mobility will decrease. This will reduce the ON-current of M2, such that the NAND gate might no longer meet the timing requirements when the clock is turned back on.
- The electron mobility will increase. This will increase the ON-current of M2, improving the speed of the NAND-gate when the clock is turned back on.
- The threshold voltage will decrease (increase in absolute value). This will reduce the ON-current of M2, such that the NAND gate might no longer meet the timing requireme ✔ when the clock is turned back on.
- The threshold voltage will increase (decrease in absolute value). This will increase the ON-current of M2, improving the speed of the NAND-gate when the clock is turned back on.

Maximum marks: 6

14



Fill in the blanks in the text below. Words are suggested for each blank – choose the most appropriate one. (correct: 1p, wrong: -0.5p, blank: -0.5p, minimum score: 0p)

Consider an NMOS transistor where the source and bulk terminal are connected to grund, as illustrated above. If the gate voltage is gradually increased from zero volt, negative charges will be induced in the underlying Si. For low gate voltages, the induced negative charge is dominated

by Select alternative (electrons in the inversion layer formed under the gate, ionized donors, ionized acceptors, mobile electrons). When the gate voltage is further increased, the

concentration of Select alternative (ionized donors, electron-hole pairs, mobile electrons, ionized acceptors) in a thin surface region under the gate will increase rapidly, forming a conductive channel between the source and drain terminal. When the gate voltage reach

the *threshold voltage* V_T, Select alternative (a current can flow between the drain and source terminal, a significant current will flow through the gate due to quantum tunneling effects., the concentration of mobile electrons in the channel equals the concentration of mobile holes in the substrate, the current will be essentially unchanged if the gate voltage is increased even further).

The transistor is now said to be operating in Select alternative (weak inversion, the linear region, strong inversion, saturation).

If a positive voltage is applied to the drain terminal, a current will flow from drain to source. This

current is dominated by Select alternative (diffusion, velocity saturation, drift,

recombination) of Select alternative (electron-hole pairs, holes, electrons). Because of the

positive drain voltage, the concentration of mobile charge carriers is Select alternative

(lowest at the drain-end of the channel, dominated by ionized acceptors, independent of the gate voltage, highest at the drain-end of the channel) and the channel resistance is

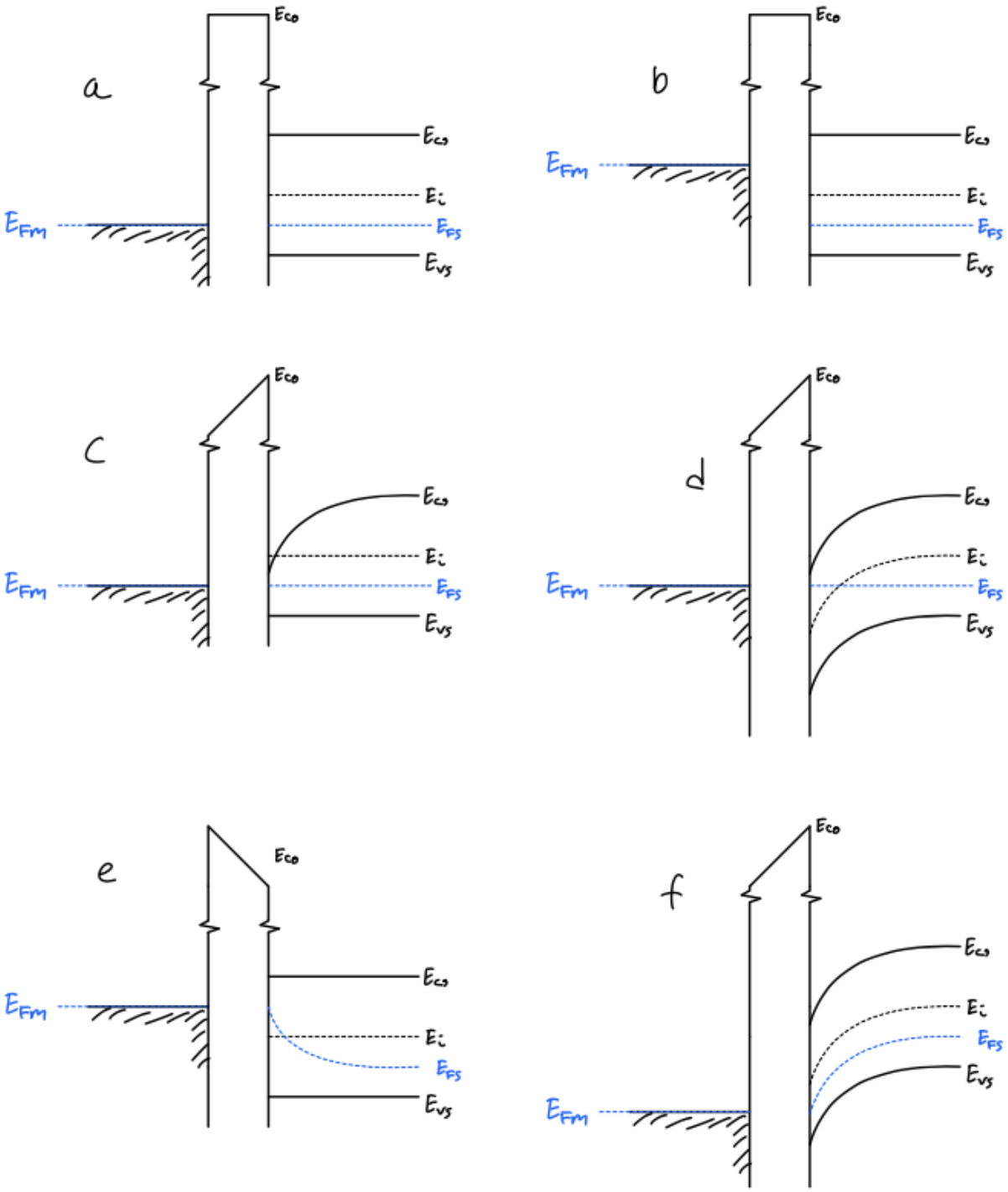
Select alternative (highest at the source-end of the channel, zero if the gate voltage is higher than the threshold voltage, highest at the drain-end of the channel, essentially the same

throughout the channel). The electric field along the channel is Select alternative (strongest in the middel of the channel, constant throughout the channel, strongest at the drain-end of the channel, strongest at the source-end of the channel) such that the drain current is

Select alternative (highest at the source-end of the channel, zero, constant, highest at the drain-end of the channel).

Maximum marks: 10

15 The figure shows different illustrations of the band diagram of a MOS structure. Which of the illustrations shows a plausible band diagram for a real MOS capacitor?
(correct: 1p, wrong: -1p, blank: 0p, minimum score: 0p)

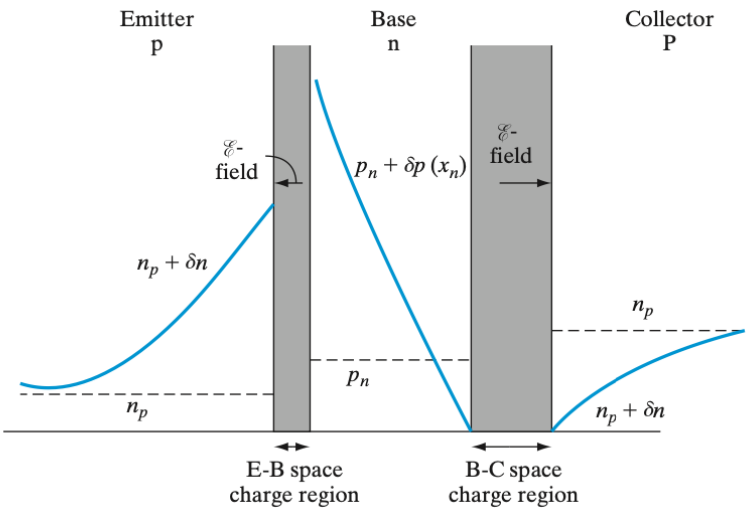


Select one or more alternatives:

- [ ] d ✔
- [ ] f
- [ ] b ✔
- [ ] e
- [ ] c
- [ ] a ✔

Maximum marks: 3

16



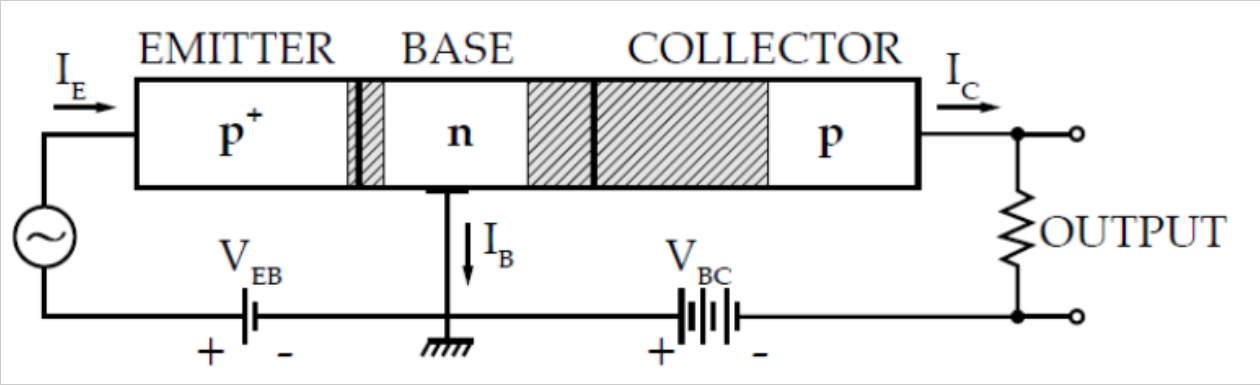
The figure above shows the minority carrier distributions of a PNP bipolar junction transistor (BJT) in the normal active mode. The hole concentration at the emitter- and collector-end of the base region is Δp_E and Δp_C, respectively, the width of the neutral base region is W_b, the cross-section area of the BJT is A and the minority carrier lifetime in the base is τ_p.

Assuming $\delta p_n(x_n)$ is linear in the base region, what is the expression for the base current?
(correct: 4p, wrong: 0p, blank: 0p)
Select one alternative:

- $I_B = \frac{qA\Delta p_E W_b}{\tau_p}$
- $I_B = \frac{qA\Delta p_E W_b}{2\tau_p}$ ✔
- $I_B = \frac{qAL_p\Delta p_n}{\tau_p}$
- $I_B = qA\frac{D_p}{L_p}\left[(\Delta p_E + \Delta p_C)\tanh\frac{W_b}{2L_p}\right]$

Maximum marks: 4

17



For the BJT shown above, which relationship between the doping concentrations agrees with the sketch:
(correct: 2p, wrong: 0p, blank: 0p)

- $N_E < N_B > N_C$
- $N_E < N_B < N_C$
- $N_E > N_B > N_C$ ✔
- $N_E > N_B < N_C$

What is the operation mode of the BJT shown above:
(correct: 2p, wrong: 0p, blank: 0p)

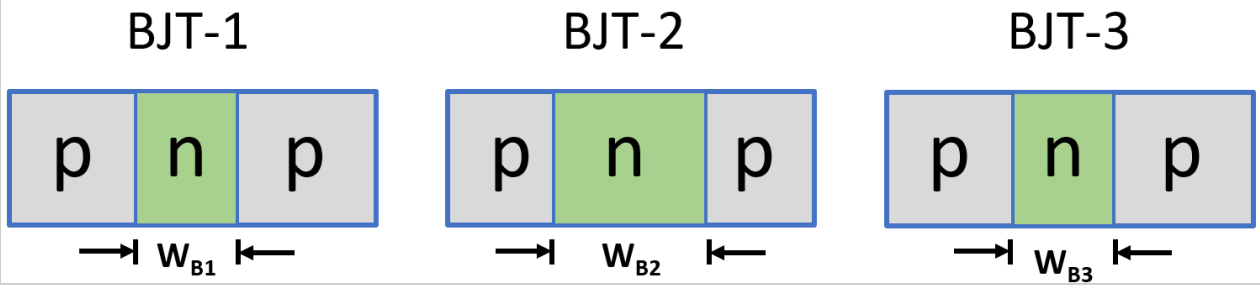
- Cutoff
- Saturation
- Inverted
- Normal active ✔

What is the the biasing arrangement shown above called:
(correct: 2p, wrong: 0p, blank: 0p)

- Coupled-diode
- Common emitter
- Common base ✔
- Gummel-Poon

Maximum marks: 6

18



The three p-n-p bipolar junction transistors schematically illustrated above, are identical except that BJT-2 has a base region that is twice as wide as that of BJT-1 and BJT-3. We also have that BJT-3 and BJT-2 have a doping in the base region that is twice as large as that of BJT-1. That is:

$W_{B2} = 2W_{B1} = 2W_{B3}$ and $N_{B3} = N_{B2} = 2N_{B1}$

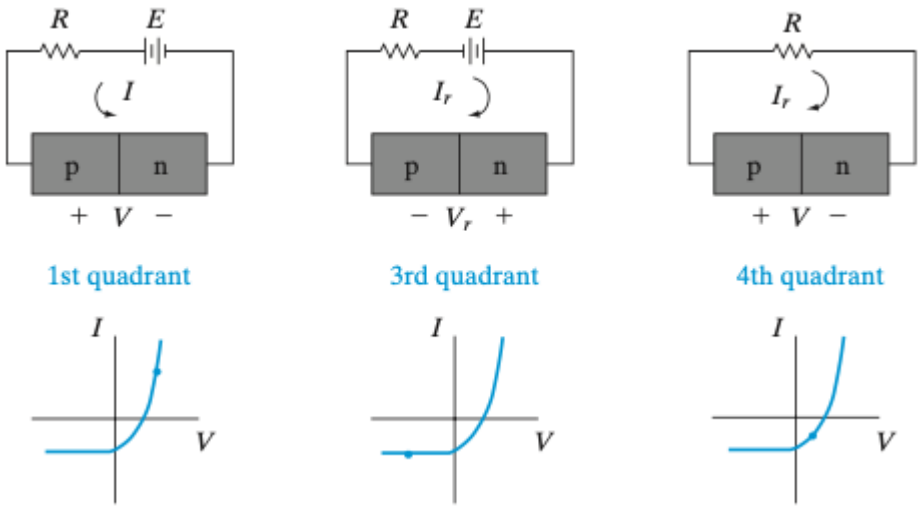
We assume that $N_E > N_B > N_C$ for all three transistors.
(correct: 1p, wrong: -1p, blank: -1p, minimum score: 0p)

Which of the three transistors will have the highest value for:

	BJT-3	BJT-1	BJT-2
Emitter injection efficiency	○	✔	○
"Punch-through" voltage	○	○	✔
Base transport factor	○	✔	○
Common emitter gain	○	✔	○

Maximum marks: 4

19 The figure below shows a p-n junction operated in the various quadrants of its I-V characteristic.



(correct: 1p, wrong: -1p, blank: -1p, minimum score 0p)

Select which quadrant the junction should be operated in, when it is to be used as a solar cell, photodetector and a LASER.

	4th quadrant	1st quadrant	3rd quadrant
LASER	○	○ ✔	○
Photodetector	○	○	○ ✔
Solar cell	○ ✔	○	○

Maximum marks: 3

20

InsperaScan (30 p.)

Problem a-e gives 6p each

Maximum marks: 30

ℹ Formulas

ℹ Constants and conversions

Electrostatic discharge

Electrostatic discharge (ESD) is the phenomena where an electrostatic voltage spontaneously discharges as an electrical current impulse. In a typical work environment, a charge of about 0.6µC can be induced on a body capacitance of 150µF, leading to electrostatic potentials of 4000 V or greater. Any contact by the charged human body with a grounded object, such as an integrated circuit (IC) pin, can result in discharge currents of several amperes, potentially causing significant damage to the IC. In the design of ICs, it is therefore common practice to include an ESD protection circuit, protecting the internal circuits from ESD currents.

A typical context of an ESD protection circuit is shown if figure 1. A pin is used to interface with an integrated circuit. When a normal signal, e.g. a logical high voltage, is applied to the pin, we want the current to flow into the circuit. However, in the case of an ESD event, we want the high ESD current to flow directly to ground through the ESD protection circuit, thereby leaving the circuit undamaged.

A standard solution to this problem, is the so-called grounded-gate NMOS (GGNMOS), shown in figure 2. A sketch of the cross-section is shown in figure 3.

a) Draw a similar cross-section and indicate the border of the depletion regions when the drain voltage (i.e. the pin voltage), V_D, is

   i) 0V

   ii) 1.5V

b) When the PIN voltage is 1.5V, only a small leakage current will flow to ground through the drain-bulk junction of the GGNMOS.

   i) Give an expression for the leakage current density (current per area).

   ii) Will the current through the drain-bulk junction be dominated by holes or electrons?

   iii) Show that the leakage current will increase with increasing temperature.

c) When an ESD event occurs, the PIN voltage of 1000V will cause a reverse brakedown in the drain-bulk junction. Will this be a Zener brakedown or an avalanche breakdown? Justify your answer.

d) Calculate the conductivity in the substrate when the doping concentration is $N_A = 10^{14}\text{cm}^{-3}$. Assume $\mu_n = 1350\text{cm}^2/\text{Vs}$ and $\mu_p = 480\text{cm}^2/\text{Vs}$.

e) The breakdown current will flow through the substrate to the p^+ region, which forms an ohmic contact to a metal wire connected to ground. Due to the finite conductivity in the lightly p-doped substrate, there will be an increased potential in the substrate, which will cause the source-bulk junction to become forward biased. This will "turn on" the parasitic NPN bipolar transistor consisting of the source (emitter), substrate (base) and drain (collector) regions.

   Sketch and explain the flow of electrons and holes in this NPN transistor when it operates in the normal active mode. Let the thickness of the arrows indicate the relative size of the current components.

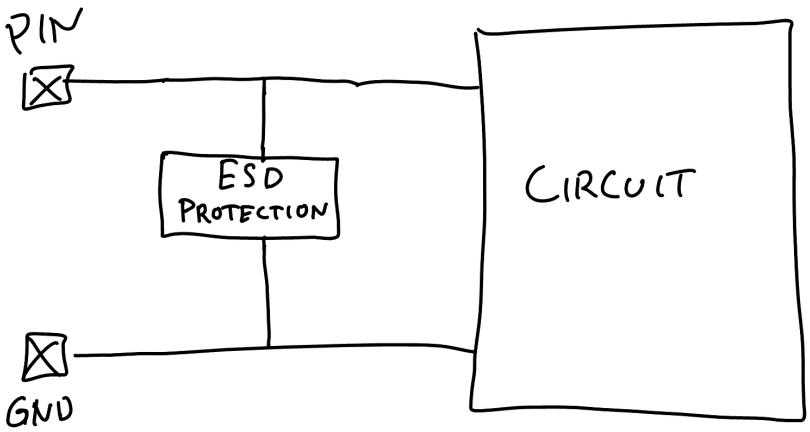


Figure 1: The context of an ESD protection circuit

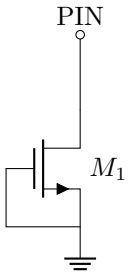


Figure 2: Circuit schematic of the grounded gate NMOS

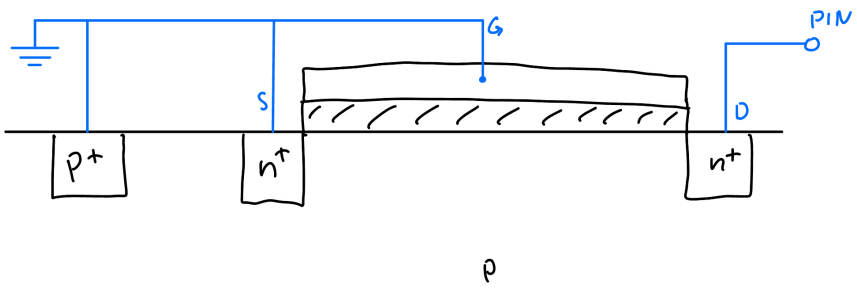


Figure 3: Sketch of the cross-section of a GGNMOS.

ESD Problem - solution

a) See figure 1

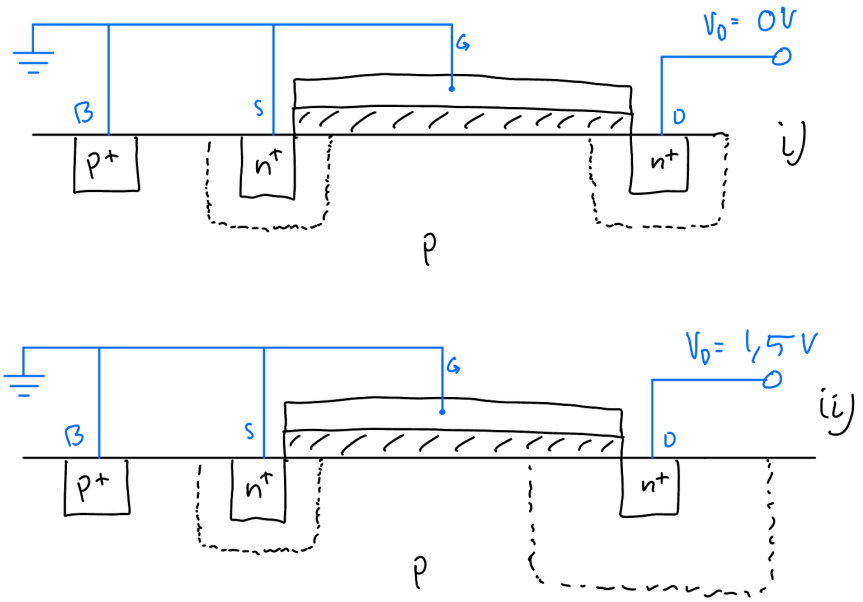


Figure 1: A cross-section indicating the border of the depletion regions when the drain voltage is 0V and 1.5V.

b) i) The leakage current will be the reverse-bias current of the n^+-p junction between the drain and the substrate, given by

$$I_0 = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)\left(e^{qV_D/kT} - 1\right) \approx -qA\left(\frac{D_n}{L_n}n_p\right), \tag{1}$$

as $V_D >> kT/q$ at room temperature and $n_p >> p_n$.

ii) As thís is a n^+-p junction, the current will be dominated by electrons.

iii) Let N_A denote the doping concentration in the substrate. By assuming $p_p = N_A$ and using the mass-action law, we get

$$I_0 = -qA\left(\frac{D_n}{L_n}\frac{n_i^2}{N_A}\right). \tag{2}$$

As n_i increases with temperature (see (3-26) in formula sheet), we see that the leakage current will also increase with temperature.

c) This will be an avalanche breakdown because Zener breakdown only happens in junctions with heavy doping on both sides.

d) As $N_A >> n_i$ we assume $p_p = N_A$ and therefore

$$n_p = \frac{n_i^2}{p_p} = \frac{(1.5 \cdot 10^{10}\text{cm}^{-3})^2}{10^{14}\text{cm}^{-3}} = 2.25 \cdot 10^6\text{cm}^{-3} \tag{3}$$

Using (3-43) we find the conductivity as

$$\sigma = q(n_p\mu_n + p_p\mu_p) = 7.68 \cdot 10^{-3}\Omega^{-1}\text{cm}^{-1} \tag{4}$$

e) See figure 2. When the NPN transistor enters the normal active mode, the forward biased source-bulk junction injects a huge amount of electrons into the substrate, which moves towards the drain by diffusion. They are swept across the reverse biased drain-bulk junction by the strong electric field and leaves the drain terminal as the main part of the ESD current.

The hole current has three contributions. The main component is the base current, caused by recombination of electrons in the substrate. Some holes will flow through the forward biased source-bulk junction and the rest will drift to ground through the ohmic p^+ contact.

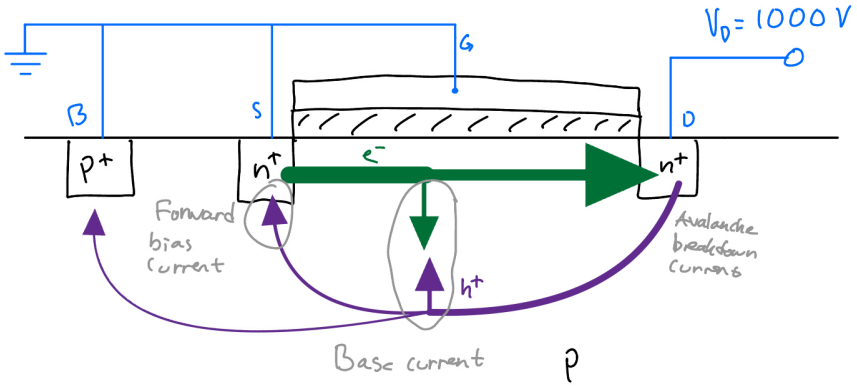


Figure 2: A sketch of the flow of electrons and holes in the NPN transistor when it operates in the normal active mode. The thickness of the arrows indicates the relative size of the current components.